

FORM PTO-1449 (SUBSTITUTE) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT (37 CFR 1.98(b))				Attorney Docket No.: PEK-In1137 Appl. No.: Applicant: JOSEF FAZEKAS ET AL. Filing Date: August 25, 2003 Group Art Unit:			
EXAMINER INITIALS		PATENT NO.	DATE	PATENTEE	CLASS	SUB CLASS	FILING DATE
<i>SR</i>	A	5,777,486	7/7/98	Hsu			
	B						
	C						
	D						
	E						
	F						
	G						
	H						
	I						
FOREIGN PATENT DOCUMENT							
		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB CLASS	TRANSL. YES NO
<i>SR</i>	J	06077299	3/18/94	Japan			
<i>SR</i>	K	2000003947	1/7/00	Japan			
<i>SR</i>	L	2000174085	6/23/00	Japan			
<i>SR</i>	M	0 448 273 A1	9/25/91	Europe			
	N						
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)							
<i>SR</i>		Schafft, H. A.: "Reliability Test Chips: NIST 33 & NIST 34 for JEDEC Inter-Laboratory Experiments and More", 97 IRW Final Report, pp. 144 and 145					
<i>SR</i>		Sriram, T. S.: "Electromigration Test Structure Designed to Identify via Failure Modes", IEEE, 2000, pp. 155-157					
EXAMINER <i>Shourang Hu</i>				DATE CONSIDERED <i>8/16/04</i>			